Test Application

Device Driver

Hardware Abstraction Layer

Hardware RTL

Software Layers

FGPA Gates and CLB

FPGA Development Board

Hardware Layer

A screenshot of a computer program

Description automatically generated

main () function

Platform (UART, GPIO, Interrupt) initialization

Bootloader code

Test initialization function

Actual Testcase

main () function

Platform (UART, GPIO, Interrupt) initialization

Bootloader code

SPI IP configured in Loopback mode

Load SPI\_FIFO with test data and trigger the Transfer

Data integrity test and printing the log

Exit test and platform deinit

main () function

Platform (UART, GPIO, Interrupt) initialization

Bootloader code

SPI IP config and Flash Init

Load SPI\_FIFO with test data and trigger the Transfer and Read back the data

Data integrity test and printing the log

Exit test and platform deinit

Write Enable

(0x06)

Sector Erase

(0xD8)

Get Status

(0x05)

Write Enable

(0x06)

Page Program

(0x02)

Random Read

(0x03)

Processor

(Micro blaze)

BRAM

(256kB)

SYS TIMER

GPIO

UART

DEBUG SS

SYSTEM

BUS

DUT

AXI

AXI

AXI

AXI

AXI

AXI

Interrupt Controller

AXI

IRQ lines

Clock & Reset SS

Debug lines

Clock & Reset

PLATFORM SS

DUT SS

OSC CLK

RESET

PWM IO

GPIO [1:0]

UART IO

SPI IO